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**1** [Delay extraction-based passive macromodeling techniques for transmission line type interconnects characterized by tabulated multiport data](#)
[Andrew Charest](#), [Ram Achar](#), [Michel Nakhla](#), [Hsuan Erdin](#)

 August 2009 **Analog Integrated Circuits and Signal Processing** , Volume 60 Issue 1-2

**Publisher:** Kluwer Academic Publishers

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This paper introduces a novel algorithm for delay extraction-based passive macromodeling of multiconductor transmission line type interconnects characterized by multiport (Y, Z, S, or H) tabulated parameters. The algorithm determines a unique logarithm ...

**Keywords:** High-speed interconnects, Hybrid parameters, Macromodeling, Measurements, Tabulated data, Transmission lines

**2** [A delay measurement method using a shrinking clock signal](#)
[Jae Wook Lee](#), [Ji Hwan Chun](#), [Jacob A. Abraham](#)

 May 2010 **GLSVLSI '10: Proceedings of the 20th symposium on Great lakes symposium on VLSI**
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This paper describes a delay measurement method using a shrinking clock signal. The shrinking clock is generated from an AND operation on two clock signals having slightly different periods, which are provided by an external tester. Instead of measuring ...

**Keywords:** delay, edge placement accuracy, measurement, tester

**3** [Minimum delay optimization for domino logic circuits---a coupling-aware approach](#)
[Ki-Wook Kim](#), [Seong-Ook Jung](#), [Taewhan Kim](#), [Sung-Mo Kang](#)

 April 2003 **Transactions on Design Automation of Electronic Systems (TODAES)** , Volume 8 Issue 2

**Publisher:** ACM [Request Permissions](#)

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Minimum delay associated with the hold time requirement is of concern to circuit designers, since race-through hazards are inherent in any multiple clock organization or clock distribution tree irrespective of clock frequency. The monotonic property ...

**Keywords:** Logic synthesis, coupling, delay minimization, domino logic

**4** [Extracting RTL models from transistor netlists](#)
[K. J. Singh](#), [P. A. Subrahmanyam](#)

 December 1995 **ICCAD '95: Proceedings of the 1995 IEEE/ACM international conference on Computer-aided design**
**Publisher:** IEEE Computer Society

 Full text available: [Publisher Site](#) , [Pdf](#) (119.32 KB) Additional Information: [full citation](#), [abstract](#), [references](#), [cited by](#), [index terms](#)
**Bibliometrics:** Downloads (6 Weeks): 4, Downloads (12 Months): 14, Downloads (Overall): 326, Citation Count: 3

This paper addresses the problem of deriving a register-transfer level (RTL) model from a transistor-level circuit. Using existing techniques, the transistor-level circuit is converted into a relation that describes the evolution of the signals in the ...

**Keywords:** Formal verification, Extraction, RTL model, Switch-level simulation

**5** [Evolutionary Synthesis of Arithmetic Circuit Structures](#)
[Takafumi Aoki](#), [Naofumi Homma](#), [Tatsuo Higuchi](#)

 December 2003 **Artificial Intelligence Review** , Volume 20 Issue 3-4

**Publisher:** Kluwer Academic Publishers

Full text available:  [Publisher Site](#)Additional Information: [full citation](#), [abstract](#), [references](#), [cited by](#), [index terms](#)**Bibliometrics:** Downloads (6 Weeks): n/a, Downloads (12 Months): n/a, Downloads (Overall): n/a, Citation Count: 3



This paper presents an efficient graph-based evolutionary optimization technique called Evolutionary Graph Generation (EGG), and its application to arithmetic circuit synthesis. Key features of EGG are to employ a graph-based representation of individuals ...

**Keywords:** arithmetic circuits, circuit design, evolutionary computation, evolutionary design, genetic algorithms, genetic programming, multiple-valued logic

## 6 [At-speed boundary-scan interconnect testing in a board with multiple system clocks](#)

 [Jongchul Shin, Hyunjin Kim, Sungbo Kang](#)
January 1999 **DATE '99**: Proceedings of the conference on Design, automation and test in Europe**Publisher:** ACMFull text available:  [Pdf](#) (200.12 KB)Additional Information: [full citation](#), [references](#), [cited by](#), [index terms](#)**Bibliometrics:** Downloads (6 Weeks): 1, Downloads (12 Months): 11, Downloads (Overall): 74, Citation Count: 3

## 7 [Simultaneous impulse stimulation and response sampling technique for built-in self test of linear analog integrated circuits](#)

 [Wimol San-Um, Tachibana Masayoshi](#)
August 2009 **SBCCI '09**: Proceedings of the 22nd Annual Symposium on Integrated Circuits and System Design: Chip on the Dunes**Publisher:** ACM  [Request Permissions](#)Full text available:  [Pdf](#) (2.12 MB)Additional Information: [full citation](#), [abstract](#), [references](#), [index terms](#)**Bibliometrics:** Downloads (6 Weeks): 1, Downloads (12 Months): 24, Downloads (Overall): 24, Citation Count: 0

This paper proposes a new impulse stimulation and response sampling technique for the implementation of a Built-In Self Test of linear analog integrated circuits embedded in mixed-signal systems. The testing technique is the monitoring of physical fault ...

**Keywords:** built-in self test, impulse stimulation, linear analog integrated circuits, response sampling technique

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